BIDIRECTIONAL LATERAL SUPERJUNCTION DEVICE WITH RESURF REGION

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/406,386, filed August 27, 2002 and U.S. Provisional Application No. 60/408,518, filed September 4, 2002.

[0002] This application is related to application Serial No. 09/891,727, filed June 26, 2001.

FIELD OF THE INVENTION

[0003] This invention relates to semiconductor devices and more specifically relates to lateral conduction and bidirectional conduction superjunction devices.

BACKGROUND OF THE INVENTION

[0004] MOSFET superjunction devices are well known and are disclosed in U.S. Patent 4,754,310 and 5,216,275 and in a publication entitled "Simulated Superior Performance of Semiconductor Superjunction Devices" by Fujihara and Miyaska in the Proceedings of 1998 International Symposium on Semiconductor Devices & ICs, pages 423 to 426. Such superjunction devices have required deep trenches or sequentially deposited and diffused P and N epitaxially layers of silicon for their production.

[0005] Superjunction devices also frequently employ deep spaced pillars of semiconductor material of one conductivity in a substrate of the opposite conductivity type. The total charge of the pillars is matched to that of the surrounding substrate in which they are received to enable the use of a high

concentration substrate which has a reduced R_{DSON} in forward conduction, while blocking is obtained by equally depleting out charge from substrate and pillars. A conventional DMOS gate structure is used to turn the device on and off.

[0006] It would be desirable to make a superjunction device of simpler structure to enable the use of a simpler manufacturing process than that used to form the deep spaced pillars; and to make a device that can be bidirectional and capable of blocking voltage applied to either the source or drain, relative to the other terminal. It would also be desirable to have such a device which does not require a termination structure.

BRIEF SUMMARY OF THE INVENTION

[0007] In accordance with the invention, a novel device structure which is symmetric and in which the source and drain terminals are interchangeable is provided. The source and drain terminals are placed within regions which are capable of supporting high reverse voltage as well as possessing low resistivity. Current flow in the channel region which is between these regions is controlled by a gate electrode.

[0008] In a first embodiment, the device employs laterally extending parallel spaced vertical trenches with sidewall diffusions which are easily fabricated.

[0009] In a second embodiment, lateral interleaved layers of N and P materials and a trench gate are used. The layers can be formed by successive depositions of N or P epitaxial silicon, each layer being diffused with the opposite conductivity type. No masking is needed for these steps, and no termination structure is needed. Thus, the semiconductor drift region comprises alternate N-type and P-type regions one on top of the other to allow high voltage blocking during the blocking mode while permitting low resistance to current flow during the conduction mode.

[0010] In a bidirectional embodiment, capable of blocking voltage applied to either the drain or source terminal relative to the other, the device structure

is symmetric in which the source and drain terminals are interchangeable. The source and drain terminals are placed within regions which are capable of supporting high reverse voltage as well as possessing low resistivity. A gate electrode controls current flow into the drift region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is a cross-section through a small section of the active area of a wafer after the etching of trenches therein in a process to make a device in accordance with the disclosure of copending application Serial No. 09/891,727 (IR-1698).

[0012] Figure 2 is a cross-section of the area of Figure 1 after the formation of an N^- implant in the trench walls and bottom.

[0013] Figure 3 is a cross-section of Figure 2 after the grooves are filled with oxide.

[0014] Figure 4 is a cross-section like that of Figure 3 after the deposition of oxide over the full upper surface of the active area and is a cross-section of Figure 5 taken across section line 4-4 in Figure 5.

[0015] Figure 5 is a cross-section of Figure 4 taken across section line 5-5 in Figure 4.

[0016] Figure 6 is a top view of the wafer of Figures 4 and 5, showing the main electrode for a plurality of devices integrated into a common chip.

[0017] Figure 7 and Figure 8 are similar to Figures 4 and 5 respectively.

[0018] Figures 9 and 10 show a second embodiment of the structure of Figure 7 and 8 which eliminates the intermediate N type epi layer of Figures 7 and 8.

[0019] Figures 11 and 12 show the structure of Figures 7 and 8 in which an oxide insulation layer is used in place of the N type epi layer of Figures 7 and 8.

[0020] Figure 13 is a cross-section of a small portion of a chip or die made in accordance with the invention.

[0021] Figure 14 is a cross-section of Figure 1 taken across section line 14-14 in Figure 13, showing two adjacent ones of the plural spaced trenches of the device.

[0022] Figure 15 is a cross section of a small portion of a superjunction chip mode in accordance with the invention and using a single gate.

[0023] Figure 16 is a schematic representation of Figure 1 with particular relevant process detail added.

[0024] Figures 17A and 17B are diagrams showing the operation of the device of Figures 15 and 16 in the on state and off state respectively.

DETAILED DESCRIPTION OF THE DRAWINGS

[0025] To place the embodiments of the present invention in perspective, the structure of the lateral superjunction device disclosed in copending application Serial No. 09/891,727 (IR-1698) is first described in connection with Figures 1 to 12.

[0026] Referring first to Figure 1, there is shown a small portion of the active area of a wafer 10 of silicon which is to be processed to form a lateral superjunction device. Wafer 10 may have a very lightly doped P^{--} main body 11 of float zone material. A very lightly doped epitaxial layer of N^{--} silicon 12 is grown atop layer 11. P^{-} region 13 is next epitaxially grown atop the N^{--} region 12.

[0027] For a 600 volt device, the P^{-} region 11 may have a concentration of about 2E14 of any desired P type impurity. The N^{--} region 12 may have a concentration corresponding to a dose of 1E12 of a suitable impurity species, thus forming a RESURF dose. The P^{-} region 13 has a concentration corresponding to a double RESURF dose of 2E12 of a suitable P type impurity.

[0028] As further shown in Figure 1, a plurality of parallel laterally elongated trenches 20 to 23 are formed through the P^{-} region 13 and into the top of

N^- region 12. The trenches may be of any length, depending on the desired breakdown voltage of the device, and, for a 600 volt device, may be about 40 microns long. The mesa width, that is, the space between trenches, may be about 1.0 microns and the trenches may be about 5 microns deep and about 0.5 microns wide. The trenches preferably extend into N^- region 12 for about 0.15 microns. To obtain the desired RESURF dose for the above sized mesa, a P^- concentration of 2E16 ions/cm^3 should be used.

[0029] After forming trenches 20 to 23, and as shown in Figure 2, the walls of the trenches receive an N^- diffusion 30 which produces a RESURF diffusion of equivalent dose of 1E12/cm^2 along the bottoms of the trenches. In order for the structure to work properly, the depth of P^- diffusion 30 and the depth of the trench should be close to one another, and, below the trench, the P concentration should drop to the amount required to support 600 volts (the BV voltage) in the bulk, which is about 2E14 ions per cm^3. One way to achieve this is to control the concentration of the P deposit in the mesas is by diffusion from the sidewalls. The doping could also be achieved by diffusion from a doped film or by bombardment with a doped plasma.

[0030] As next shown in Figure 3, a suitable dielectric, for example, silicon dioxide 35, fills in the trenches by thermal growth or by deposition.

[0031] As next shown in Figures 4 and 5, a MOSgate structure is formed (in any desired sequence) and the source and drain electrodes are also formed. More specifically, the MOSgate structure may include a conventional P^- 40 which contains an N^+ source 41. A P^+ diffusion 42 may also underlie the source region. The center of the source/base structure receives a shallow etch which is later filled by source electrode 43. A conventional gate oxide 44 covers the lateral invertible channel between the source 41 and the lightly doped portion of base 40 regions and a conductive polysilicon gate electrode 50 overlies the gate oxide. An insulation layer 51 of low temperature oxide, for example, insulates gate electrode 50 from the source metal 43.

[0032] As next shown in Figure 5, an N^+ sinker 60 extends from the top of P^- region 13 to N^- diffusion 30 and the N^- region 12. The top of regions or mesas 13 receives a field oxide 61 (Figures 4 and 5) which has an opening there through to receive drain contact 62 which contacts N^+ sinker 60.

[0033] Figure 6 shows a topology which can be used for the structure of Figures 4 and 5, where a plurality of separate but repeating elements are formed which each laterally adjacent source and drain regions S_1 to S_4 and D_1, D_2 have the same structures as shown in Figures 4 and 5. The source regions S_1 to S_4 may be for separate integrated devices, or alternatively, may be connected together and, similarly, drains D_1 and D_2 may be separate or connected together. Gate electrodes G_1 to G_4 may also be located adjacent sources S_1 to S_4 respectively and are connected to their respective gate electrodes such as gate electrode 50.

[0034] The operation of the device of Figures 4 and 5 is as follows:

[0035] In the blocking mode, and when source 43 and gate 50 are grounded with respect to substrate 12, and a high relative bias is applied to drain 62, the voltage in the lateral direction is supported entirely in the trench structure, and P^- regions 13 and N^- diffusions 30 fully deplete, allowing an almost uniform electric field distribution along the trench length. This depletion region extends downwardly into N^- region 12.

[0036] In the conduction mode of operation, and with the application of a bias to gate electrode 50 and the grounding of source 43 relative to substrate 12, an N type channel is formed between source regions 41 and base 40. The application of a bias to drain 60 will cause a current to flow in the device through the undepleted P^- and N^- regions 13 and 30.

[0037] Referring next to Figures 7 to 11, the structure of Figures 4 and 5 is duplicated in Figures 7 and 8 so that it can be easily contrasted to the two additional embodiments of Figures 9, 10 and Figures 11 and 12 respectively. The same numerals are used throughout to identify similar components.

[0038] Referring to Figures 9 and 10, there is shown a simplified arrangement compared to that of Figures 4, 5, 7 and 8 which eliminates the N^- region 12 of Figures 7 and 8. Thus, the source 41 and substrate 11 are shorted so the device cannot withstand voltage (preventing its use as a high-side switch). However, the device of Figures 9 and 10 withstands voltage between the drain 60 and the source electrode by the resurf principle.

[0039] Referring next to Figures 11 and 12, an oxide insulation layer 70 is used in place of N^- region 12 and the active area is formed on the surface of layer 70. Thus, the device, unlike that of Figures 7 and 8, can be used as a high-side switch.

[0040] The first embodiment of the invention is shown in Figures 13 and 14 and is a modification of the structure of Figures 7 to 12 to produce a bidirectional conduction device.

[0041] In Figures 13 and 14, semiconductor substrate 100 upon which the device is formed is a high resistivity P-type substrate (preferably about 50 ohm.cm). All conductivity types hereinafter described can be reversed. A P type implant or an epitaxial layer 101 is grown atop substrate 100 to any desired thickness with a concentration of impurity atoms (boron for example) of $1x10^{16}$ per cm^3. A further P type implant is performed upon substrate 101 to create a P-type region 104 (Figure 13) doped to about $1X10^{17}$ cm^{-3}. This is required to obtain the desired threshold voltage for conduction. A plurality of trenches 102 (Figure 14) each of which is 5 micron deep, about 0.5 micron wide, and spaced from one another (into the plane of the paper) by 0.5 micron apart, and are about 85 to 90 microns long are then etched into P region 104 and penetrate into the substrate 101 beneath region 104. The trenches 102 are in one half of the device and are interrupted by a gap 120 to define trench sections 102A and 102B (Figure 13). The sidewalls and bottoms of each of these trenches receive N-type diffusions 116 while the mesa regions 117 between the trenches remain P-type. The doses in the N regions 116 and P mesas 114 is such that the cumulative doping in all regions 117 and 116 is N-type.

[0042] The trenches 102A and 102B are filled with a dielectric 115 such as a silicon dioxide. The space 120 between the groups of trenches 102A and 102B constitutes the invertible channel whose conductivity can be modulated by the application of bias to the gate electrode 131 which is separated from the channel by the gate oxide 132. High dose, low energy implants are then performed in the central regions of these trench groups 102Aand 102B to form shallow, extremely low resistivity source regions 140 and drain regions 141. Ohmic contacts 142 and 143 are made to these regions 102A and 102B, respectively. The trench groups 102A and 102B are passivated by means of a suitable dielectric film 150. Electrical contact to the semiconductor substrate is provided a back-side metallization 151.

[0043] Blocking Operation of Figures 13 and 14:

[0044] When the source 142 and gate 131 are grounded with respect to the substrate contact 151 and a high relative bias applied to the drain contact 143, the voltage in the lateral direction is supported entirely in the 40 micron long trench 102B with minimal depletion in the channel region 104, allowing reduced channel lengths. This is due to the RESURF effect where the N-type implants 116 and the mesa doping 117 in trenches 102B laterally deplete out completely, allowing an almost uniform electric field distribution in the entire group 102B. Directly below the drain implant region 141, a punchthrough N^+NP^- diode is present and the applied bias is supported mainly in the P^- region with the depletion region extending about 40-50 microns into the substrate. The potential at the bottom of the deep trenches 102B is highest below the drain 141 and reduces gradually, moving away from drain region 141 towards the periphery of group 102B, reducing to near zero at a distance of about 40 microns from region 141. This contours the depletion region in the substrate and acts as a self-termination.

[0045] Conduction Operation of Figures 13 and 14:

[0046] With the application of a bias to the gate electrode 131 and the grounding of the source 142 with respect to the substrate 151, an N-type channel is formed on the surface of channel 104. The application of a small bias to the drain

143, 141 will cause a current to flow in the device. At this low bias the trench regions 102A and 102B are not depleted and hence the current can flow from the drain metal 143 into the region 141 and then into the sidewalls 116 in group 102B and then into surface channel 104 and then into the sidewalls 116 in group 102A and finally into the source region 140 and into the source metal 142. The use of the RESURF principle allows the resistivity of the trench sidewalls 116 to be substantially less than that of a plane parallel drift region capable of supporting the same blocking voltage.

[0047] A second embodiment of the invention is shown in Figures 15, 16, 17A and 17B for a geometry in which the interleaved layers are parallel to the surface of the wafer or chip which receives the devices. Thus, Figures 15 and 16, show a cross-section of a chip of the invention which requires no critical mask step for its fabrication and requires no termination. Further, the device of Figures 15 and 16 is a undirectional conduction embodiment, which can be easily made bidirectional by creating a symmetrical gate structure.

[0048] In Figures 15 and 16 semiconductor substrate 201 upon which the device is formed is a high resistivity P^- type substrate (preferably about 50 ohm.cm). A region 202 comprising alternating N-type and P-type layers are then provided on the top surface of substrate 201 either by means of epitaxy or ion implantation or their combination. Each layer of region 202 has a dose of approximately 1E 10^{12} cm^{-2} and is approximately 0.5 to 1.0 micron thick. A relatively low resistivity N-type region 203 is created at one end of structure 202, extending through to region 201. Grooves such as groove 207 are etched into the top surface of region 202, extending into substrate 201, and separated from region 203 by a pre-determined distance of, for example, approximately 45 microns. Grooves 207 are lined with a gate oxide 204. The region 202 on the opposite side of groove 207 from region 203 maybe be doped P^- to about 1E 10^{12} cm^{-2} up to a desired depth to create the P^- body region 205 and to fix the threshold voltage. A conductive gate electrode 206 (conductive polysilicon) is provided in trench 207 separated from region 202 by a gate oxide 204. The semiconductor surface between the P body

region 205 and the gate oxide 204 constitutes the device channel whose conductivity can be modulated by the application of bias to the gate electrode 206.

[0049] High dose low energy implants are then performed in the top surface of regions 205 and 203 to form shallow, extremely low resistivity source regions 304 and drain regions 309. The layers 202 are passivated by dielectric layers 403 and 404 (such as TEOS or the like) which insulate gate electrode 206 and source and drain electrodes 300 and 301 respectively from region 202. Electrical contact to the semiconductor substrate is provided with a backside metallization 302.

[0050] It should be noted that the structure of Figures 1 and 2 can be made bidirectional, simply by adding a second gate structure symmetric with gate 206.

[0051] The operation of the device of Figures 1 and 2 is as follows considering the diagrams of Figures 17A and 17B. First considering operation in the blocking condition (Figure 17B) where the source 300 and gate 206 are grounded with respect to the substrate 201 and a high relative bias applied to the drain 301, the voltage in the lateral direction is supported entirely in the 45 micron long epitaxial region 202. The sidewalls of the grooves 207 facing region 203 are held to a potential close to that of the substrate by the formation of conducting PMOSFETs on that sidewall. The region 202 depletes out completely allowing an almost uniform electric field distribution along its length. Directly below the drain implant region 203 (Figure 15), an N^+NP^- diode is present and the applied bias is supported mainly in the P^- region 201 with the depletion region extending about 40-50 microns into the substrate. The potential at the bottom of region 202 is highest below the drain 203 and reduces gradually moving away from region 203 towards the grooves 204, reducing to near zero at a distance of about 45 microns from drain 203. This contours the depletion region in the substrate and acts as a self-termination.

[0052] Considering next the operation in the conduction mode (Figure 17A), with the application of a bias to the gate electrode 206 and the grounding of the source 304-300 with respect to the substrate 201, an N-type channel

is formed on the channel surface 208. The application of a small bias to the drain 203-301 (Figure 15) will cause a current to flow in the device. At this low bias the regions 202 are not depleted and hence the current can flow from the drain metal 301 into the region 309 (Figure 15) and then into the region 202 and then around the groove 207 into surface channel 208 (Figures 15 and 17A) and then into the source region 304 and into the source metal 300. The use of the RESURF principle allows the resistivity of the layers 202 to be substantially less than that of a plane parallel drift region capable of supporting the same blocking voltage. Thus, the device conducts with very low on resistance.

[0053] To summarize these operations which are schematically illustrated in Figures 17A and 17B; in the on state, as shown in Figure 17A, electrons are conducted from the source and around the side and bottom of groove 204. In the off state, as shown in Figure 17B, it will be noted that:

1. The hole layer electrically connects the P regions of epitaxial regions 202 to the substrate 201;

2. The N layers of region 202 are tied to the high potential of the drain; and

3. The full length of region 201 uniformly depletes out.

[0054] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.